Comparing, Contrasting and Interpreting Data For Test Socket Signal Integrity Performance

Selecting a test socket based on its published bandwidth may not give an accurate representation of the product's real-world performance. When comparing the signal integrity performance of test sockets, it's important to consider several factors, as this article explains.

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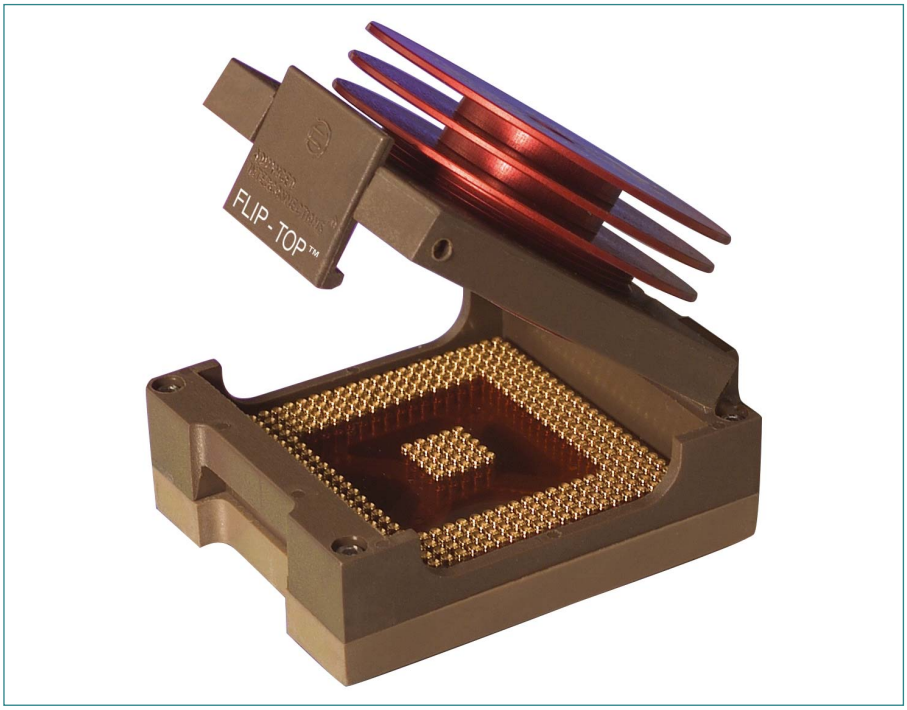

Figure 1. This is an example of a surface mount test socket for a ball grid array-packaged device.

Because there are several factors involved in determining a test socket's actual signal integrity (SI) performance, the use of published bandwidth alone may not represent the true picture.

Signal Fidelity

Understanding how the intrinsic attributes of the test socket itself affect signal fidelity and determining that the published results are based on a properly conducted SI study (test methodology) will help ensure that a test socket performs as expected.

Knowing the basic elements of a thorough SI characterization study and being able to recognize the limiting factors of signal integrity performance will aid in comparing and interpreting test socket performance data published by competing manufacturers.

A paramount consideration when selecting a test socket is to ensure that the transmission-line characteristics of the test socket meet or exceed those of the chipset (see Figure 1).

Avoiding 'False-Positive' Results

If they are poorly matched, a receiving device may never receive (or recognize) signals sent from the chipset, thereby causing an inadvertent system failure. Armed with a basic understanding of SI fundamentals, test socket users can avoid this "false-positive" test result.

How DNA Affects Signal Integrity

Just like a fingerprint, each test socket has its own unique set of signal integrity performance metrics.

Because test sockets are normally more capacitive than inductive, we can now consider how the DNA of a test socket influences the electromagnetic coupling between adjacent socket terminals.

When reviewing SI data, the socket user should examine two key SI parameters: the insulative material's dielectric constant and its loss tangent (dissipation factor).

Just like a fingerprint, each test socket has its own unique set of signal integrity performance metrics.

The signal fidelity of each socket is essentially predetermined by the confluence of its raw materials—terminal geometry, plating, and centerline distance—the socket's DNA, so to speak.

In a given system environment, this DNA will manifest itself as quantifiable signal integrity performance attributes that define how well or how poorly a test socket will perform electrically within that system.

Dielectric Constant

The dielectric constant is a measure of a material's relative effectiveness to act as an electrical insulator. It is expressed as a unitless numerical value and is used to compare materials in terms of their relative dielectric loss values. Suffice it to say the more "lossy" a material, the less insulative and more conductive it will be.

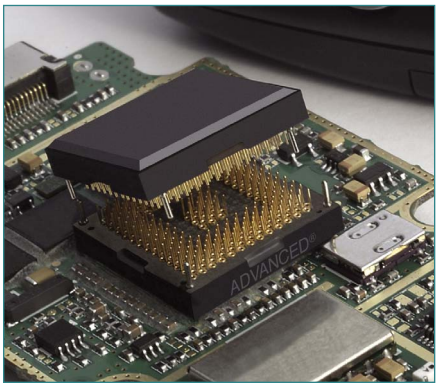

Figure 2. Socket adapter systems are used for test validation when PC board space is constrained.

The dielectric loss tangent is a measure of the rate of loss of electric power in a dielectric material, usually in the form of heat. The dissipation factor is dependent upon the current flowing through the terminals of the socket and is expressed as the ratio of resistive elements to the capacitive elements within the electrical path.

Much like dielectric constants, loss tangents with low values result in a "fast" signal transmission medium, while loss tangents with high values result in a "slow" medium.

Scattering Parameters

Terminal geometry will greatly affect the return loss and insertion loss (scattering parameters) as well as other SI performance attributes such as resistance, inductance, capacitance, impedance, and cross-talk.

It would be an ideal SI situation if the terminals were of a uniform cross-section for their entire electrical length. However, in most cases this is not possible, since socket terminals are specifically shaped and formed to provide areas for device engagement, areas that capture it within the insulative material, and areas suitable for surface mount or plated-through-hole solder reflow processes, to name a few.

Consequently, each change in shape and cross-section along the electrical length of the terminal introduces a change to the SI attributes of that section. As such, the impedance of each section is different.

Impedance Mismatch

These changes in impedance cause an "impedance mismatch" to occur, resulting in a portion of the propagated signal being reflected back to its source.

If this mismatch is large enough, the voltage within the terminal decreases to a value that dictates when little or no power will flow through the terminal.

At elevated frequencies, the surface finish of the socket terminals and the electrical conductivity of their plating also contribute to the overall SI performance of a test socket, due to a phenomenon known as the "skin effect."

As the frequency increases, current flow will be concentrated near the outer surface or "skin" of a terminal, creating the path on which signal transmission occurs. Therefore, test socket terminals with superior surface finish and plating will demonstrate better SI performance than those terminals without those attributes.

Terminal Spacing

The last item that affects SI performance is terminal spacing. When comparing test socket data, the user should remember that increasing or decreasing the proximity of a terminal with respect to other terminals in an array will affect certain SI attributes.

In one example, increasing the distance between adjacent terminals will have a net effect of decreasing crosstalk and mutual capacitance while increasing impedance.

Alternatively, if the distance between adjacent terminals is decreased, crosstalk and mutual capacitance will increase and impedance will decrease.

Characterization Methodology

Test sockets are typically complex, multi-component structures comprising one or more insulative dielectric materials and one or more conductive elements to channel voltage, power, and—in certain instances—electromagnetic parasitics.

In this discussion, electrical path length is limited to the physical extent of the test socket's electrically conductive terminals, and excludes all signal integrity artifacts of the PWB's surface mount pads and vias.

Of particular interest within SI are the scattering parameters, or "S-parameters," which represent the reflection and transmission coefficients of a propagated signal.

For the purpose of this discussion, S-parameters are captured to describe the behavior of a test socket under linear conditions over a bandwidth of DC to 20GHz (see Figure 3).

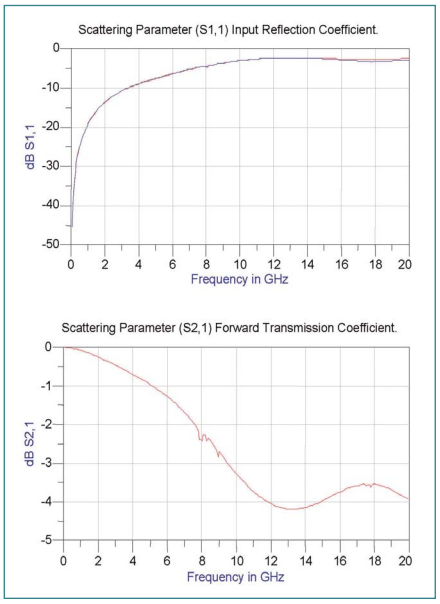

Figure 3. S-parameters may be used to quantify the reflection and transmission coefficient of a propagated signal.

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Why Select S-Parameters?

The advantage of selecting S-parameters as the foundation for SI characterization is not limited to its complete description of the test socket's performance; it also

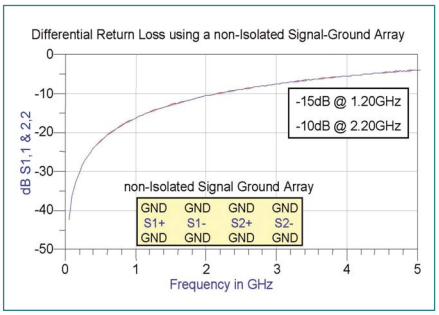

Figure 4. Non-isolated differential array showing the true effect of S1,1 on adjacent signal conductors.

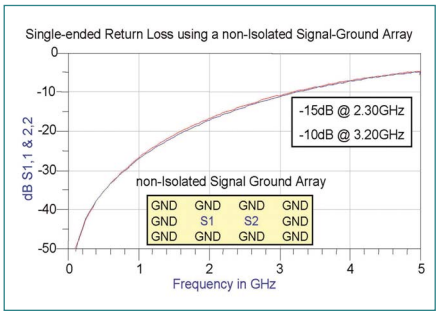

Figure 5. Non-isolated single-ended array showing the true effect of S1,1 on adjacent signal conductors.

provides the ability to study other performance metrics that indicate the socket's signal fidelity.

Examples include impedance, near-end and far-end crosstalk, resistance, inductance, capacitance and eye diagrams. Additionally, SPICE and IBIS model extractions are made possible. S-parameters are voltage ratios of the transmitted wave, typically stated in decibels at a given frequency and designated as follows:

S-parameter	Description
S1,1	*Input reflection coefficient*
S2,1	*Forward transmission coefficient*
S1,2	*Reverse transmission coefficient*
S2,2	*Output reflection coefficient*

Simply stated in SI terminology, the S-parameters *S1,1* and *S2,2* are known as the return loss (reflection) and can be described as the loss of signal power transmitted to an electrical load due to an impedance mismatch that causes a portion of the transmitted signal to be reflected back to its source.

Attenuation

The S-parameters *S1,2* and *S2,1* are known as the insertion loss (attenuation), described as the loss of signal power and voltage due to dissipation or absorption by an electrical load in the circuit.

As passive devices, most test sockets are normally more capacitive than inductive; it is this capacitance that influences return loss performance, which ultimately determines the upper limit of the socket's operational bandwidth.

When end users evaluate the insertion loss performance of the socket, it is important only to discern its signal attenuation with respect to the frequency dictated by the socket's return loss.

Frequency Domain Vs. Time Domain

Utilizing a state-of-the-art vector network analyzer (VNA) makes it quite convenient to conduct signal integrity studies in the frequency domain.

The VNA creates a closed-loop system environment that allows the broadband response of a test socket to be characterized over a specific bandwidth. As an example, one may wish to characterize a test socket over a DC to 20GHz bandwidth with an emphasis on quantifying the transmitted signals scattering parameters, particularly *S1,1* (the reflection coefficient) and *S2,1* (the transmission coefficient).

As a general rule, frequency domain studies may be routinely applied except where the time domain extractions of impedance and crosstalk are more applicable. Because of its importance, the balance of this article will be devoted to the electronic characterization of test sockets in the frequency domain.

As a general rule, frequency domain studies may be routinely applied except where the time domain extractions of impedance and crosstalk are more applicable.

Test sockets must perform in numerous applications involving signals that are propagated in either single-ended mode or differential mode, while being subjected to the negative influence of common-mode signals.

A properly conducted test socket study will characterize transmission line performance in both single-ended and differential modes.

Common-Mode Signals

The study should also take into account the effects of the naturally occurring common-mode signals. signals. These are normally signal fidelity inhibitors traveling in the opposite direction, which propagate through the second terminal of the pair.

Single-ended versus differential signaling modes are considerably different. In single-ended mode, a signal is propagated through a single electrical path-in this instance, the terminal of a test socket.

In differential mode, signals are propagated through a pair of test socket terminals as follows: Signal 1 propagates through one terminal of the pair and Signal 2 (theoretically equal to Signal 1 and traveling in the opposite direction) propagates through the second terminal of the pair.

Interpreting and Comparing SI Data

One method of ensuring that an accurate and realistic electronic characterization of a test socket will be achieved is to pay close attention to the signal and ground assignments designed into the test PWBs.

Special care must be given to establishing the proper test patterns that will be used to either simulate or measure signal integrity data.

Whether in differential or single-ended mode, specific test patterns must be implemented for each mode to properly capture the scattering parameters of the test socket while examining other performance attributes. (See Figures 4 and 5.) These

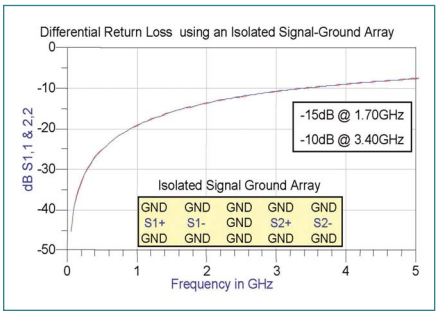

Figure 6. Isolated differential array showing the non-influenced effect of S1,1 on adjacent signal conductors.

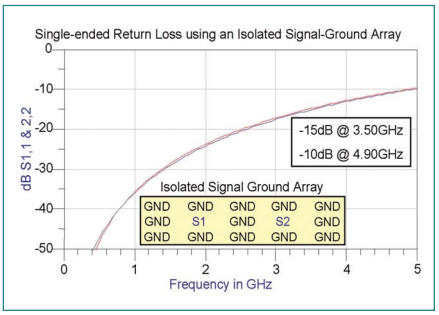

Figure 7. Isolated single-ended array showing the non-influenced effect of S1,1 on adjacent signal conductors.

include, but are not limited to, impedance, near-end and far-end crosstalk, resistance, inductance, capacitance, eye-diagrams and SPICE and IBIS model data.

Workers skilled in the signal integrity discipline understand that the judicious orientation and placement of signal versus ground terminals will have a profound effect on the accuracy and realistic quality of any simulated or measured signal integrity data.

Certain arrays of signal and ground terminals dispersed within an insulative dielectric medium will display more favorable signal fidelity than other arrays. Therein lies the dilemma most digital designers and systems engineers encounter: They are faced with the task of selecting a test socket from one of several manufacturers.

This process normally involves a comparison of signal integrity data generated using disparate methods, signal-to-ground ratios, and test patterns.

Comparisons Difficult

Those grappling with this dilemma know full well that not all signal integrity testing and reporting are created equal; consequently, the data is not equivalent, making comparisons between sources very difficult.

It is therefore incumbent upon the end user of test sockets to identify the signal-to-ground ratios and testing patterns reported by the various sources first.

One must ensure that superior signal fidelity has not been achieved by the use of an unrealistic terminal array—which, in our opinion—is one that isolates aggressor and victim terminals from each other by introducing ground terminals between them (see Figures 6 and 7).

This testing method, in fact, will usually skew the performance data of the socket in a more favorable direction. This practice creates a "best case" socket scenario that in all likelihood will not serve the needs of most systems engineers and digital designers, because an unrealistic number of terminals must be assigned to ground to achieve the reported socket performance.

Conclusion

This article offers an abridged overview of a complex discipline to help test socket users understand how the combination of materials, geometry, and test methods affect SI performance and reporting.

In the absence of a uniform standard of practice for SI characterization, adhered to by all test socket manufacturers, design engineers are faced with a comparison dilemma.

Armed with a basic understanding of both SI terminology and the impact of a socket's intrinsic attributes on SI performance, design engineers must then look at the methodology employed by each socket manufacturer to ensure that published results are consistent and in line with real-world applications.

Most test socket users will tend to favor data that is in line with their own decision-making processes, likely preferring an extremely aggressive signal-to-ground ratio.

This typically includes aggressor and victim terminals that are not isolated from each other, but instead are exposed to the adverse effects of adjacent electromagnetic coupling and common-mode signals. This approach would be more representative of an actual digital environment.

Signal Integrity characteristics generated by this practice will more accurately address the socket user's I/O assignments (netlist) and help to determine where best to run high- versus low-frequency signals through a test socket.

Furthermore, this practice will yield unbiased SPICE and IBIS models that would enable system designers to create and debug a net list quickly and accurately.

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